FDM Evaluations

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FDM Resonators: Physical size, bandwidth, uniformity

Short description: Current 68x chips are 42.605 x 93.11 mm with 68 resonances between ~ 1.6 – 5.3 MHz. Smaller chips would help with overall size of readout components in the cryostat as well as potential thermal contraction issues. Both inductor and capacitor contribute similarly to physical size. Expanding the bandwidth used (including to lower frequencies), will enable higher multiplexing factors. Uniformity of fabrication within a chip can impact yield if resonances overlap. Chip-to-chip uniformity could impact crosstalk.

	Evaluation	Rationale
Cost		Reducing size could allow more resonators on a single 6” wafer (currently 2 sets of 68), reducing total number of wafers needed & fabrication cost. Increasing bandwidth & multiplexing factor could also reduce # of wafers in production (but would require R&D investment that would lessen this).
Schedule		Reducing total number of chips would impact wafer fabrication schedule linearly. Wire-bonding time would remain the same. Changing physical size would not impact schedule.
Science (Stat)	1	Same number of channels will be wired with or without changes. Smaller size could mitigate a potential failure mode of the chips due to thermal contraction (preserving yield).
Science (Sys)	3	Improved control over peaks in the comb will mitigate intramodule crosstalk, currently measured to be median level of 0.22% between nearest neighbors with outliers (see Avva JLTP 2018). What is our crosstalk requirement?
Target completion date		
Estimated Investment		0.5 FTE fab, 0.5-2 FTE design/ testing. Design, modeling, testing and iteration . Minimum of 3 batches of iteration required, $20-30k for fab alone depending on material choice.
Likelihood of success	1-2	
Added Risks/Challenges		Changing size significantly requires new method for making LC resonators or different component values. Expanding to fully utilized warm electronics bandwidth requires additional work on & verification of high-frequency noise (see noise slide). Further expansion requires additional re-design of warm electronics. Ability to achieve smaller features (line & separation) is driving factor here, and use of latest industry-developed techniques.

FDM: Production rate & cost of resonator assembly (no wiring)

Short description: Current 68x chips are produced 2 per wafer in batches of 15 wafers. Current production requires deposition of superconducting film (either aluminum or niobium) at outside company and lithography, liftoff, and dicing in-house . Assembly requires gluing chip to PCB board, wire-bonding of chips (~15 min per 2 chips). SPT-3G focal plane required 14 batches of resonators, and 240 total chips. Chip production rate was 8 months for full set. Cost of single batch is ~$9K for Nb, ~$4.5K for Al.

	Evaluation	Rationale
Cost		Streamlining fabrication would reduce cleanroom /tool time. Baseline materials cost will depend on # of wafers, and thus would stay the same. Would different batch sizes make sense?
Schedule	2	Limiting factor in full production will be testing & validation of resonator assemblies.
Science (Stat)	1	Same number of channels will be wired with our without development here.
Science (Sys)	1	Production does not impact systematic effects.
Target completion date		
Estimated Investment		
Likelihood of success	2	

FDM: Multiplexing Factor

Short description: Current multiplexing factor for FDM is 68. Limitations include: resonator physical size (for using lower bandwidth), crosstalk (for packing factor within a given bandwidth), parasitic impedances (impacts noise performance at higher end of bandwidth). Resonance width is dictated by TES stability criterion. Other limitations are the dynamic range of the SQUID (as size of error signals grow), and dynamic range of DACs that are providing the voltage biases & feedback.

	Evaluation	Rationale
Cost		Ideally, increasing the multiplexing factor would reduce the number of modules required and thus cost. However, there may be other changes required (different warm components, different chip size, etc) that would increase it again. Evaluating cost savings in this case is not possible without a detailed proposal. Cost is primary driver for increasing mux factor. One estimation of potential savings.. Increasing from 68 to 300x for 300,000 detectors: SQUIDs: $1M, custom stripline wiring: $0.25M, resonators: $1.4M assuming still fit 2 modules/600 resonators per 6" wafer, warm electronics: if same architecture is possible with 8 modules /2400 channels per FPGA then reduced number of boards would save up to $3.5M.
Schedule		See above.
Science (Stat)	1	Same number of channels will get wired with our without this change, not a performance driver . Could enable FDM to work with wafers of more tightly packed detectors (i.e. higher observing band).
Science (Sys)	1	Increased multiplexing permutates how crosstalk might be introduced… crosstalk within a single module is a measured effect.
Target completion date		
Estimated Investment		
Likelihood of success	2	No laboratory implementation of higher multiplexing modules.
Added risks/challenges		As multiplexing factor increases, faulty modules impact more detectors. How much of an increase in multiplexing factor can current warm electronics support (FPGA signal processing, voltage bias, nulling). Error signal through SQUID will grow with increased multiplexing factor as well. At what point does this become a problem?

FDM: Noise (low freq, white)

Short description: The readout noise level directly impacts the instrumental sensitivity and mapping speed. There are two aspects of FDM noise worth consideration (A) First 2018 on-sky results from SPT-3G instrument are consistent with photon noise dominated performance. However, these results do not fully agree with detailed laboratory measurements, which demonstrate that the readout noise level can be further suppressed. Optimization of both readout and detector parameters can result in improved readout noise. (B) The contribution of readout to the total noise budget could be lowered beyond the current theoretical expectation. Readout noise level is a combination of noise from room-temperature components (DACs, amplifiers, resistors), intrinsic SQUID noise, and bias resistor noise. Reducing the noise contribution from any of these components at the 1-2pA/rt(Hz) level could roughly impact the total *readout* contribution by 10%. Changes to the overall design of the cryogenic system could also produce noise improvements. One readout noise component scales with frequency due to current division at the SQUID input. Reducing the responsible strays would enable use of high-frequency bandwidth (see reducing parasitics). Finally, readout noise is referred to noise equivalent power on the sky by the detector voltage bias. Reducing voltage bias can reduce noise.

	Evaluation	Rationale
Cost		There is no construction cost savings in improving the noise. Would reduce operations cost (i.e., better/expected noise performance = less observing time for same science outcome).
Schedule	1	R&D on the noise will not improve the fabrication & assembly timeline.
Science (Stat)	3-4	Detailed evaluation of noise in SPT-3G deployed instrument is underway and more details will be provided in the future, but see intro above. Reducing the median readout noise contribution by a further ~ 10% as stated above, with various assumptions bolo properties (for a range of loading but with current voltage bias levels) improves the mapping speed by roughly 6%. Reducing voltage bias levels would result in further significant improvements.
Science (Sys)	1	Noise level only impacts statistical.
Target completion date		
Estimated Investment		
Likelihood of success	3	Performance of small-scale lab system does not always cleanly map to full-scale instrument.
Added Risks/Challenges		Any change to room temperature components to reduce theoretical noise level would require full system validation. Challenge in getting the last 10% can require full system & environment. System integration needs to be robust, including clear designs for filtering, grounding, and power supply. Effect of readout noise on NEP is also closely linked to detector bias voltage, can be either an opportunity or a risk.

FDM: Reduce parasitics, move SQUID to cold stage

Short description: Parasitic contributions in the wiring, connections in the FDM cryogenic circuit alter the current flow from the ideal design, impacting both systematics and noise. Reducing the parasitic inductance of wiring between the resonators and SQUID will reduce a source of crosstalk, however, it will also negatively impact the current sharing and noise as a function of frequency. Reducing the parasitic SQUID input coil inductance will reduce the current sharing and flatten the noise as a function of frequency. Reducing parasitic series resistance from resonator chip (LC) would improve detector stability. Parasitic inductance in series with the bias resistor alters the voltage bias across the bolometer. Dependent on the implementation, other strays in the system can create undesirable resonances in the active bandwidth. Changes to the cryogenic wiring setup could also improve the effective multiplexing factor in units of (channels)/(heat load).

	Evaluation	Rationale
Cost		If successful, main cost savings will be due to the lack of highly custom superconducting wiring (~12k for order of 60 pieces, although it is expected this would scale different at higher order values). Assuming 68x across 100,000 detectors (1470 modules) this corresponds to 120k (although wiring is still required and would reduce this savings).
Schedule	2-3	Attachment of the wiring currently requires specialized methodology. Current fastest technician assembly is 2 hours per set of 8 modules. Total estimated time ~ 16 days minimum (of 24 hour work).
Science (Stat)	2	Same number of detectors will be connected with our without these changes. Moving SQUID to cold stage could reduce its contribution to the total noise budget. Reducing series parasitics enables low-R detectors and lower bias voltage, reducing readout NEP.
Science (Sys)	3	Reduced parasitic will mitigate wiring impedance crosstalk. Total crosstalk currently measured to be median level of 0.22% with outliers (see Avva JLTP 2018).
Target completion date		
Estimated Investment		
Likelihood of success	2-3	Work is ongoing, but still in the early stages (no laboratory demonstration yet).
Added risks/challenges		Verification of the noise performance in the suggested scenario will be required over the full bandwidth, as removing the parasitic will exacerbate a known noise multiplication as a function of frequency.